This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (canceled)

2 (currently amended): ~~The~~ A non-volatile semiconductor device ~~according to claim 1,~~ comprising:

a memory cell array having electrically erasable programmable non-volatile memory cells;

a plurality of reprogramming and retrieval circuits that temporarily store data to be programmed in the memory cell array and sense data retrieved from the memory cell array, each reprogramming and retrieval circuit having a first latch and a second latch, the first latch being connected to a selected bit line of the memory cell array via a first transfer switch and a second transfer switch series-connected to each other, the second latch being connected to a connection node of the first and the second transfer switches via a third transfer switch, a data node of the second latch being connected to data input and output lines via column selection switches; and

a controller that controls the reprogramming and retrieval circuits on data-reprogramming operation to and data-retrieval operation from the memory cell array,

wherein, after the data has been programmed in a selected memory cell, the programmed data is retrieved for programming verification, the retrieved data being sensed and stored in the first latch.

3 (currently amended): The non-volatile semiconductor device according to claim ~~1~~2, wherein each reprogramming and retrieval circuit has a multilevel logical operation mode and a caching operation mode, in the multilevel logical operation mode, re-programming and retrieval of upper and lower bits of two-bit four-level data being performed using the first and the second latches in storing the two-bit four-level data in one of the memory cells in a predetermined threshold level range, in the caching operation mode, data transfer between one of the memory cells selected in accordance with a first address and the first latch being performed while data transfer is being

performed between the second latch and input/output terminals in accordance with a second address with respect to one-bit two-level data to be stored in one of the memory cells.

4 (original): The non-volatile semiconductor device according to claim 3, wherein in the multilevel logical operation mode, the first and the third transfer switches are turned on to connect the second latch to a selected bit line for pre-charging data stored in the second latch on the bit line.

5 (original): The non-volatile semiconductor device according to claim 3, wherein the four-level data is defined as "11", "10", "00" and "01" from lower level of the threshold level range.

6 (original): The non-volatile semiconductor device according to claim 3, wherein different row addresses are allocated to the upper and the lower bits of the four-level data for programming and retrieval.

7 (original): The non-volatile semiconductor device according to claim 6, wherein a first and a second data programming operation are performed in the multilevel logical operation mode, in the first data programming operation, the lower-bit data being loaded into the second latch and then stored in the first latch, programming being performed to a selected memory cell based on the data stored in the first latch, in the second data programming operation, the upper-bit data being loaded into the second latch and then stored in the first latch while lower-bit data already programmed in the selected memory cell is being retrieved and loaded into the second latch, programming being performed to the selected memory cell based on the data stored in the first latch in accordance with the data stored in the second latch.

8 (original): The non-volatile semiconductor device according to claim 6, wherein a first, a second and a third retrieval operation are performed in the multilevel logical operation mode, in the first retrieval operation, "0" or "1" of the upper bit being judged using a retrieval voltage applied at a control gate of a selected memory cell, the retrieval voltage being set in a threshold level range of "10" and "00" as the four-level data, in the second retrieval operation, "0" or "1" of the lower bit when the upper bit is "0" being judged using a retrieval voltage applied at the

control gate of the selected memory cell, the retrieval voltage being set in a threshold level range of "00" and "01" as the four-level data, and in the third retrieval operation, "0" or "1" of the lower bit when the upper bit is "1" being judged using a retrieval voltage applied at the control gate of the selected memory cell, the retrieval voltage being set in a threshold level range of "11" and "10" as the four-level data.

9 (currently amended): The non-volatile semiconductor device according to claim ~~1~~2, wherein each reprogramming and retrieval circuit is selectively connected to a plurality of bit lines of the memory cell array via a bit line selection switch.

10 (currently amended): The non-volatile semiconductor device according to claim ~~1~~2, wherein each reprogramming and retrieval circuit has a common signal line connected to the connection node of the first and the second transfer switches via a fourth transfer switch.

11 (original): The non-volatile semiconductor device according to claim 10, wherein each reprogramming and retrieval circuit has a temporal storing node for temporarily storing a potential at a data node of the first latch and a fifth transfer switch provided between the fourth transfer switch and the common signal line, the fifth transfer switch being controlled by the potential at the temporal storing node.

Claim 12 (canceled)

13 (currently amended): The non-volatile semiconductor device according to claim ~~1~~2, wherein a data programming cycle for a selected memory cell of the memory cell array is performed by repeatedly programming pulse application and retrieval for programming verification, in a test mode, a cell current flowing in the selected memory cell is retrieved to the input and output terminals while the data programming cycle is interrupted during which the data retrieved by the retrieval for programming verification is stored in the first latch and the second latch is inactive.

Claims 14-32 (canceled)